



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/828,983	04/21/2004	Mark Rapaich	P1997US00	6909
32709	7590	04/19/2007		
Gateway Inc Patent Attorney PO Box 2000 N. Sioux City, SD 57049			EXAMINER SCHELL, JOSEPH O	
			ART UNIT 2114	PAPER NUMBER

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/19/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No. 10/828,983	Applicant(s) RAPACH, MARK	
	Examiner Joseph Schell	Art Unit 2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 22 January 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-28 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-28 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

Detailed Action

Claims 1-28 have been examined.

Claims 1-28 have been rejected.

Response to Arguments

Applicant's arguments with respect to all claims have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 1-7, 9-10^{-15, 17-21, 23-28} are rejected under 35 U.S.C. 102(b) as being anticipated by Lin (US Patent 6,862,695).

2. As per claim 1, Lin ('695) discloses an apparatus for detecting and indicating faults on a computer motherboard comprising:

a nonvolatile memory device for storing a plurality of diagnostic instructions for detecting faults on said computer motherboard (column 2 lines 30-36, test instructions are stored in the BIOS); and

a microprocessor, coupled to said nonvolatile memory device, for, responsive to receiving an initialization signal (as shown in Figure 5a, the computer power on begins the POST), requesting and retrieving said plurality of diagnostic instructions, and executing the diagnostic instructions so as to detect faults on said computer motherboard (column 2 lines 26-35, it's referred to as "a device" but it executes BIOS instructions, thus it is a processor); and

a visual indicator coupled to and controlled by said microprocessor for providing a visual indication when a fault on said computer motherboard is detected during execution of said diagnostic instructions by the microprocessor (as shown in Figure 5a steps 504 and 505).

3. As per claim 2, Lin ('695) discloses the apparatus for detecting and indicating faults on a computer motherboard as in claim 1, wherein said visual indicator is turned on when power is applied to said computer motherboard (column 3 line 65 through column 4 line 1).

4. As per claim 3, Lin ('695) discloses the apparatus for detecting and indicating faults on a computer motherboard as in claim 1, wherein said visual indicator is turned off upon detection of a fault on said computer motherboard (column 3 lines 5-10, an error causes LED blinking).

Art Unit: 2114

5. As per claim 4, Lin ('695) discloses the apparatus for detecting and indicating faults on a computer motherboard as in claim 1, further comprising a flash circuit for flashing said visual indicator upon detection of a fault on a memory subsystem (column 3 lines 5-10).

6. As per claim 5, Lin ('695) discloses the apparatus for detecting and indicating faults on a computer motherboard as in claim 1, wherein said nonvolatile memory device stores power-on self-test diagnostic instructions and basic input and output system instructions (column 4 lines 7-10 and 12-14, BIOS are utilized during the POST, and column 4 lines 38-45, the BIOS are verified by the POST).

7. As per claim 6, Lin ('695) discloses the apparatus for detecting and indicating faults on a computer motherboard as in claim 1 wherein said visual indicator is a light emitting diode (column 4 lines 61-64).

8. As per claim 7, Lin ('695) discloses the apparatus for detecting and indicating faults on a computer motherboard as in claim 1 wherein said visual indicator is an external visual indicator (as shown in Figure 3, the LED is externally connected through an I/O port).

9. As per claim 9, Lin ('695) discloses the apparatus for detecting and indicating faults on a computer motherboard as in claim 7, further comprising an I/O port coupled

Art Unit: 2114

to said microprocessor, said microprocessor providing signals to said external visual indicator via said I/O port (as shown in Figure 3, the LED receives signals via an I/O port).

10. As per claim 10, Lin ('695) discloses the apparatus for detecting and indicating faults on a computer motherboard as in claim 1, wherein said computer motherboard includes integrated circuits mounted on said computer motherboard (as shown in Figures 6a and 6b, the POST tests RAM, BIOS and display adapter).

11. As per claim 11, this claim recites limitations found in claims 1 and 2, with the addition of "turning off said visual indicator when no faults on said computer motherboard are detected during execution of said diagnostic instructions." This claim is rejected on the same grounds as claims 1 and 2, and this new limitation is also disclosed by Lin ('695).

Lin ('695) uses a flashing LED as an indicator of component failure during a POST (as shown in Figures 5a and 5b). Eventually, the POST will complete (element 513 of Figure 5b). As shown in Figures 5a and 5b, when the POST completes without failure in any component, the testing has ceased and the LED will *not* indicate any more test results. Thus the "indicator" characteristic of the LED ceases.

Art Unit: 2114

12. As per claim 12, Lin ('695) discloses the method for detecting and indicating faults on a computer motherboard as in claim 11, further comprising the steps of:

initializing a memory subsystem (Figure 5a, POST is an initializing process because it is done before the RAM is put to use); and

flashing said visual indicator when a fault is found on said memory subsystem (Figure 5a elements 504 and 505).

13. As per claims 13-15, these claims recite limitations found in claims 5-7, respectively, and are respectively rejected on the same grounds as claims 4-7.

14. As per claims 17-18, these claims recite limitations found in claims 9-10, respectively, and are respectively rejected on the same grounds as claims 9-10.

15. As per claim 19, 20, 21, 23, 24, and 25, this claims recites limitations found in claims 11, 12, 15, 13, 14 and 17, respectively, and are respectively rejected on the same grounds as claims 11, 12, 15, 13, 14 and 17.

16. As per claim 26, Lin ('695) discloses an apparatus for detecting and indicating faults on a computer motherboard and in a memory subsystem of a computer system comprising:

an external visual indicator (see Figure 3);

a general I/O port coupled to said visual indicator (see Figure 3);

Art Unit: 2114

a flash circuit coupled to said visual indicator for flashing said visual indicator (column 4 lines 35-37, a control signal is used to control the LED flashing, this inherently requires circuitry);

a host bus for transmitting address and data signals (see Figure 3);

a nonvolatile memory device coupled to said host bus storing a plurality of diagnostic instructions, said plurality of diagnostic instructions including power-on self-test diagnostic instructions for detecting faults in said computer motherboard and in a memory subsystem (the BIOS of figure 3, also see column 4 lines 7-10 and 12-14, BIOS are utilized during the POST, and column 4 lines 38-45, the BIOS are verified by the POST);

a microprocessor coupled to said bus, to said I/O port, and to said flash circuit, said microprocessor turning said visual indicator on through said general I/O port and requesting and retrieving said plurality of diagnostic instructions upon reception of an initialization signal to start said computer system, executing said diagnostic instructions for detecting faults in said computer motherboard prior to executing said diagnostic instructions for detecting faults in said memory subsystem, turning said visual indicator off if no faults are detected in said computer motherboard, and activating said flash circuit if faults are detected in said memory subsystem (column 2 line 62 through column 3 line 11, and see Figure 5a wherein the computer power on triggers the POST and the POST tests RAM and in Figure 5b where the POST tests BIOS).

Art Unit: 2114

17. As per claim 27, Lin ('695) discloses the apparatus for detecting and indicating faults on a computer motherboard and in a memory subsystem of a computer system as in claim 26, wherein said external visual indicator is located on a panel of said computer system (column 3 line 65 through column 4 line 1).

18. As per claim 28, Lin ('695) discloses the apparatus for detecting and indicating faults on a computer motherboard and in a memory subsystem of a computer system as in claim 26, wherein said computer motherboard comprises an integrated circuit mounted on said computer motherboard (as shown in Figures 5a and 5b, the POST tests RAM, BIOS and a Display Adapter).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

19. Claims 8, 16 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin ('695) in view of BOXX Box Boxes Clever.

20. As per claim 8, Lin ('695) discloses the apparatus for detecting and indicating faults in a computer motherboard as in claim 1. Lin ('695) does not explicitly disclose the apparatus wherein said visual indicator is an internal visual indicator.

Art Unit: 2114

BOXX Box Boxes Clever is a review of a computer casing.

At the time of invention it would have been obvious to a person of ordinary skill in the art to modify the system disclosed by Lin ('695) such that when they are unneeded, the diagnostic LEDs can be concealed. This modification would have been obvious because bright LEDs can be so annoying to a casual computer user that he may attempt to manually conceal them (BOXX Box Boxes Clever, third paragraph from the end).

21. As per claims 16 and 22, these claims recite limitations found in claim 8 and are rejected on the same grounds as claim 8.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Specifically, Warchol ('435) teaches a POST with results conveyed by a LED.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph Schell whose telephone number is (571) 272-8186. The examiner can normally be reached on Monday through Friday 9AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman can be reached on (571) 272-3644. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2114

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JS



SCOTT BADERMAN
SUPERVISORY PATENT EXAMINER